Ultra Linear Switching Rectifiers (ULSRs) for high-quality regulated 3-phase AC to DC conversion

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Abstract

We present an Ultra Linear Switching Rectifier (ULSR), a regulated 3-phase AC/DC converter with an associated simple analog controller, characterized by exceptional power quality. A ULSR is wild frequency compatible, significantly exceeds the requirements on the power factor and on the limits of the reflected current harmonics imposed by DO-160, Environmental Conditions and Test Procedures for Airborne Equipment [1], and provides a very well regulated DC output with small transient responses and fast recovery times in full range of the output powers.

Motivation

The primary focus of this ongoing work is on achieving high power quality in regulated 3-phase AC to DC converters for a wild frequency input (with the AC frequencies of up to 1 kHz) over a wide range of loads (e.g., from about 10% to full power). We target the total harmonic distortions (THD) of order 1% or better, effectively unity power factor (PF), and the efficiency of 94%-95% for a 115 VAC to 270 VDC conversion. We refer to the proposed converters as Ultra Linear Switching Rectifiers, or ULSRs, due to the highly proportional relationship between their input currents and voltages, and the active solid state switching used in this topology.

The secondary focus is on achieving a well-regulated DC output, with full-range (i.e, from full power to open circuit and *vice versa*) step transient responses of less than 2% of the DC output in amplitude, and of order 1 ms in duration. This is accomplished by a very simple, robust, and fully analog controller that provides a single common gate control signal to the MOSFET switches of the ULSR power stage, and does not require any additional start-up and/or management means.

The additional ULSR requirements include reliable behavior under heavily unbalanced mains voltages, and in case of mains failure, without significant degradation of the power quality, and the ability to easily connect various ULSR converters (of the same and/or different power ratings, and powered by the same or different and non-synchronized AC generators) in parallel to increase power and/or to provide N+1 redundancy.

Idealized concept and basic operation of ULSR

Fig. 1 shows simplified diagrams of non-isolated (left) and isolated (right) versions of a ULSR. It is initially assumed that the parasitics can be ignored, switches are ideal, and the inductances and capacitances are constant.

In a ULSR, the switches operate at a constant switching frequency $f_{\rm sw}$, and *synchronously*, that is, all three of them are “on” or “off” at the same time. Further, a ULSR operates in a discontinuous conduction mode (DCM), so that the inductor currents ($I_1^\star$, $I_2^\star$, and $I_3^\star$) in each section are zero at the beginning (and, therefore, at the end) of any switching interval. The DCM requirement constraints the maximum value of the inductance L based on the output

voltage and maximum power, minimum value of the RMS of the line voltage, and the switching frequency. Also, the minimum value of the capacitance C of the virtual neutral (VN) capacitors is constrained by the requirement that the inductor currents $I_1^\star$, $I_2^\star$, and $I_3^\star$ are increasing functions of time when the ULSR switches are "on". Next, the inductance L_l of the line inductors (which would typically need to be sufficiently larger than L) needs to be properly chosen to ensure a high power factor (PF) in full range of the line frequencies (f_AC) and in a desired range of the output powers, while providing sufficient line current filtering.

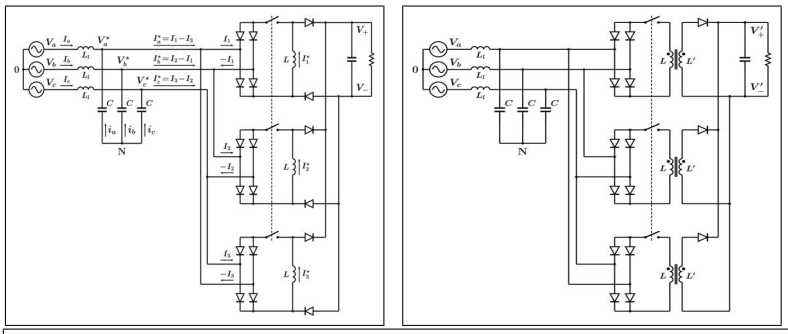

Fig. 1. Simplified diagrams of non-isolated (left) and isolated (right) ULSRs

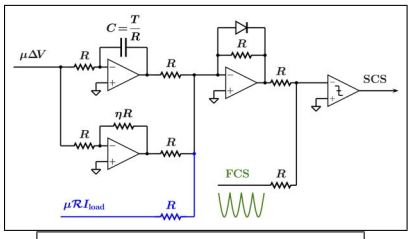

Fig. 2. Basic ULSR controller

With this, neglecting the high-frequency components, the line currents $I_a^\star$, $I_b^\star$, and $I_c^\star$ would be proportional to the respective voltages $V_a^\star$, $V_b^\star$, and $V_c^\star$. For example, $I_a^\star(t)$ can be expressed as

$$I_a^\star(t) = 3G^\star \bar{V}_a^\star(t) + \Delta I_a^\star(t)\,, \tag{1}$$

where the overbar denotes averaging over a full switching interval, $\Delta I_a^\star(t)$ is a zero-mean current with the main frequency content consisting of the harmonics of the switching frequency $\pm$ the AC frequency f_AC, and $G^\star \approx P_\mathrm{out}/(3V_\mathrm{LN})^2$ is a constant with physical units of conductance, and where P_out is the output power, and V_LN is the RMS of the line-to-neutral voltage.

ULSR controller

Fig. 2 provides an example of a basic ULSR controller circuit. The comparator outputs a logic switch control signal (SCS), turning the ULSR switches "on" with a high output, and "off" with a low output. The voltage ΔV is the difference between the output differential voltage and the desired output (reference). The component and parameter values would depend on the ULSR specifications, but the typical values would be of order $100\,\mu$s for the integrator time constant T, between 1 and 10 for the gain η, and of order 10^{-2} for the scaling constant μ.

When the frequency control signal (FCS) is a "parabolic" wave (a full-wave rectified sine wave with half of the switching frequency would be an adequate approximation), in a steady DCM state, the output of the summing amplifier would be effectively a linear function of the load current. Thus an additional current feedback (shown in blue in Fig. 2) allows approximately an order of magnitude reduction in the magnitude of the transients. The diode in the feedback of the summing amplifier limits the maximum duty cycle, and thus the maximum current drawn from the mains, during powering the ULSR on, and/or for the loads heavier than the maximum specified.

Practical considerations and mitigating effects of parasitics

The parasitic capacitances (mainly those of the power MOSFETs and the diodes) would typically result in the ULSR THD that may significantly exceed the 1% target. The main cause of these additional distortions is that the converter inductor and the parasitic capacitances of the reversed-biased bridge and output diodes, and of the open switch, form a parallel LC circuit

that would have significant residual current and voltage oscillations after the current in the converter inductor falls to zero, and thus the inductor current may not be zero at the beginning of every switching interval. As a result, the current drawn from an AC line during a switching cycle can be smaller or larger than the current drawn from the AC line when the current in, and the voltage across, the converter inductor are zero at the beginning of the cycle. This effect can be mitigated by employing active snubbers across the section inductors for a relatively short time interval (≈ 580 ns in the current prototype) at the end of a switching cycle. A typical power dissipation in a snubber in the current prototype is in a 1 W to 2 W range. Additional components (such as common mode chokes and small capacitors across the section bridges) should also be employed to reduce the effects of parasitics.

Simulated and experimental performance of the ULSR prototype

Fig. 3 shows the power factor, efficiency, and the THD of a non-isolated 3 kW 115 VAC/270 VDC developmental prototype operating at $f_{\rm SW} = 144$ kHz. The simulated power factor and the THD values have been verified, while the initial experimental power losses were approximately 15% higher than the target values, resulting in the efficiency shown by the black line in the middle panel. It is expected that the target efficiency can be attained by optimizing the parameters of the circuits mitigating the effects of parasitics. This work is underway.

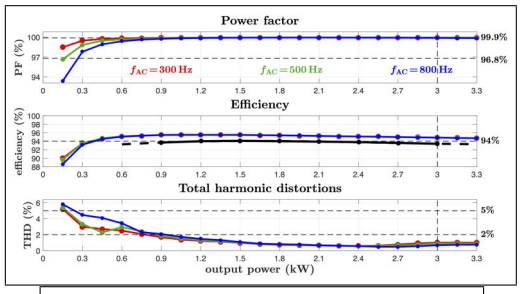

Fig. 3. Power factor, efficiency, and THD

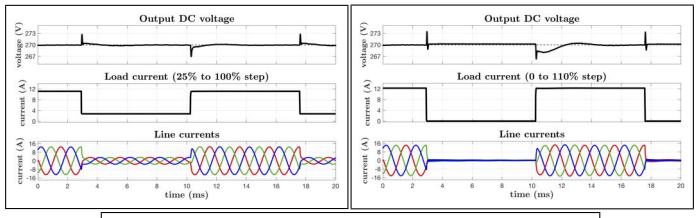

Fig. 4. Example of ULSR transient responses

Figs. 4 and 5 show the current ULSR hardware prototype (non-isolated 3 kW 115 VAC/270 VDC), and provide simulated and experimental examples of its transient responses.

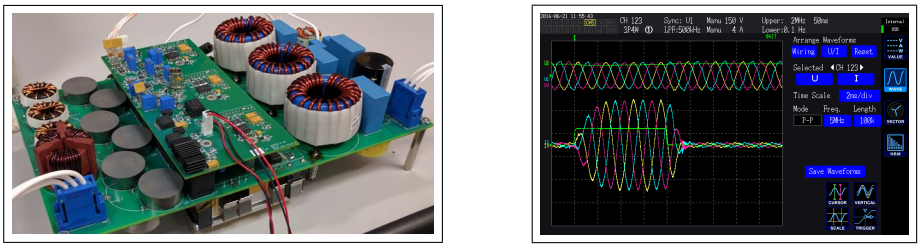

Fig. 5. 3 kW 115 VAC/270 VDC non-isolated ULSR prototype and its full-scale transients ($f_{\rm AC} = 400$ Hz)

Summary

This paper presents an Ultra Linear Switching Rectifier (ULSR), a regulated 3-phase AC/DC converter with an associated simple analog controller, characterized by exceptional power quality. The ULSR provides a very well regulated DC output with small transient responses and fast recovery times in full range of the output powers.

References

[1] "RTCA List of Available Documents, RTCA Inc." March 2013. [Online]. Available: http://www.rtca.org/Files/ListofAvailableDocsMarch2013.pdf